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**INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (Use as many sheets as necessary)		<b>Application Number</b>	
		<b>Filing Date</b>	
		<b>First Named Inventor</b>	Buchty et al.
		<b>Art Unit</b>	
		<b>Examiner Name</b>	
<b>Sheet</b> 1	<b>of</b> 1	<b>Attorney Docket Number</b>	Buchty 1-7-1

**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
st		R. ESPASA, M. VALERO, J. SMITH, Vector Architectures: Past, Present and Future, International Conference on Supercomputing (ICS'1998), pp. 425-432, July 1998	
st		Pages downloaded from home.ecn.ab.ca/~jsavard/other/arcint.htm,ar02.htm,ar0201.htm,ar0202.htm,ar020201.htm,ar0302htm,ar0304.htm; downloaded on 11/24/03	
st		P. KOOPMAN, Vector Architecture, Carnegie Mellon 18-548/15-548 Memory System Architecture, 11/4/98, downloaded from www.ece.cmu.edu/~ece548/handouts/16v_arch.pdf on 11/24/03	
st		W. BUCHHOLZ, The IBM System/370 vector architecture, IBM Systems Journal, Vol. 25, No. 1, 1986, pp. 51-62	
st		M. MITTAL, A. PELEG, U. WEISER, MMX Technology Architecture Overview, Intel Technology Journal, 3rd Quarter 1997, www.intel.com/technology/itj/q31997/pdf/archite.pdf	
st		A. PELEG, U. WEISER, MMX Technology Extension to the Intel Architecture, IEEE Micro, 1996, pp. 42-50	
st		Motorola, AltiVec Technology At-a-Glance, 2002, downloaded from http://e-www.motorola.com/files/32bit/doc/fact_sheet/ALTIVECGLANCE.pdf	
st		S. FULLER, Motorola's AltiVec Technology, 1998, downloaded from http://e-www.motorola.com/files/32bit/doc/fact_sheet/ALTIVECWCP.pdf	
st		Motorola, AltiVec Execution Unit and Instruction Set Overview, downloaded from http://e-www.motorola.com/webapp/sps/site/overview.jsp?nodeId=03C1TR0467mKqW5Nf2hG12 11/24/03	
st		V. FISCHER, M. DRUTAROVSKY, Scalable RSA Processor in Reconfigurable Hardware - a SoC Building Block, Conf. on Design of Circuits and Integrated Sys., 11/ 20-23/01, Portugal	

<b>Examiner Signature</b>	Sheng-Jun Jia	<b>Date Considered</b>	3/29/2006
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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.

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